Amendments to the Drawings

The attached sheets of formal drawings include FIGs. 1-5.

Attachment: Replacement Sheets 1-5

Remarks/Arguments

Upon entry of the accompanying amendment, claims 1 and 3-20 will be pending in this application. Claims 1-20 are rejected, and claims 16-20 are objected to in the Office Action of December 13, 2006. Claims 1, 2, 4, 5, 11, 12 and 14-20 are amended, and claim 3 is cancelled herein.

Re: Objection to Drawings

FIGS. 1 and 2 of the drawings are objected to because the Examiner asserts that the labeling of each element therein is not very clear. To rectify this matter, Applicant submits corrected drawing FIGS. 1 and 2 with this response. Withdrawal of the objection in view of these corrected drawings is respectfully requested.

Re: Objection to Claims 16-20

Claims 16-20 are objected to because of a typographical error. In particular, the term "circuit arrangement" in the preambles of claims 16-20 should read "method." Appropriate corrections are included herein and withdrawal of the objection in view of these corrections is respectfully requested.

Re: Rejection of Claims 1-4 and 14-15

Claims 1-4 and 14-15 are rejected under 35 U.S.C. §102(a or e) as being anticipated by U.S. Patent No. 6,367,079 issued to DeVos et al. (hereinafter, "DeVos"). Applicant respectfully traverses this rejection since DeVos fails to teach or suggest all elements of the claimed invention.

Applicant first notes that independent claims 1 and 15 recite:

> "a first circuit having an output line and an input line;
> a second circuit having an input line for receiving signals from the output line of the first circuit, and an output line for transmitting signals to the input line of the first circuit; and
> a control circuit for controlling signals transmitted from the output line of the second circuit to the input line of the first circuit by ***inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting***

signals to the input line of the second circuit." (emphasis added; see claim 1), and

"detecting a mode of operation of the system;
if the mode is a first mode, allowing the serial interface circuit to transmit signals to the receiver-transmitter circuit; and
if the mode is a second mode, ***detecting whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit, and if the receiver-transmitter circuit is transmitting signals to the serial interface circuit, prohibiting the serial interface circuit from transmitting signals to the receiver-transmitter circuit.***" (emphasis added; see claim 15)

As indicated above, independent claim 1 defines a control circuit that inhibits signals transmitted from the output line of a second circuit to the input line of a first circuit when the first circuit is transmitting signals to the input line of the second circuit. Similarly, independent claim 15 defines a control method that prohibits a serial interface circuit from transmitting signals to a receiver-transmitter circuit when the receiver-transmitter circuit is transmitting signals to the serial interface circuit. DeVos fails to teach or suggest this feature of the claimed invention.

In formulating the instant rejection, the Examiner alleges that: ATM interface 29 of DeVos corresponds to the claimed "first circuit" (claim 1) and "receiver-transmitter circuit" (claim 15); physical storage medium 21 of DeVos corresponds to the claimed "second circuit" (claim 1) and "serial interface circuit" (claim 15); and CPU 22 of DeVos corresponds to the claimed "control circuit" (claim 1) (see pages 3-5 of Office Action dated December 13, 2006 and FIGS. 2A and 4A of DeVos). The Examiner further alleges that "the control circuit inhibits the signals transmitted from the second circuit output line to the first circuit input line when the first circuit is transmitting signals at the output line of the first circuit," citing column 4, lines 51-62 of DeVos. With this latter allegation, the Examiner further states: "[d]uring write-in operations, element 21 is not allowed to transmit any data" (see discussion of claim 3 on page 4 of Office Action dated December 13, 2006).

In response, Applicant notes that the foregoing allegations and cited passage of DeVos do not anticipate or render obvious independent claims 1 and 15. First, Applicant points out that the cited passage of DeVos (column 4, lines 51-62) simply states:

> "A software program for write-in operation is down-loaded from the system manager 60 to the RAM 24 of the SMU 20 before copy operation of the video data is performed. The CPU 22 of the SMU 20 controls write-in operation of the physical storage medium, 21 according to the software program for write-in operation stored in the RAM 24. Then the software program for write-in operation in the RAM 24 is replaced with a software program for read-out operation by down-load from the system manager 60 before video service starts. The CPU 22 controls read-out operation of the physical storage medium 21 according to the software program for read-out operation in video service."

As indicated above, the cited passage of DeVos nowhere states that CPU 22 (the alleged "control circuit" of claim 1) inhibits signals transmitted from the output line of physical storage medium 21 (the alleged "second circuit" of claim 1) to the input line of ATM interface 29 (the alleged "first circuit" of claim 1) when ATM interface 29 is transmitting signals to the input line of physical storage medium 21. Rather, the cited passage of DeVos is completely silent regarding the signal transmission capabilities of physical storage medium 21 when ATM interface 29 is transmitting signals to physical storage medium 21. Accordingly, the Examiner's bald allegation that "[d]uring write-in operations, element 21 is not allowed to transmit any data" (see discussion of claim 3 on page 4 of Office Action dated December 13, 2006) is completely without support. For this reason alone, the instant rejection should be withdrawn. Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 1-4 and 14-15.

Re: Rejection of Claims 5-8, 10, 12-13 and 16-18

Claims 5-8, 10, 12-13 and 16-18 are rejected under 35 U.S.C. §103(a) as being unpatentable over DeVos in view of Applicant's admitted prior art. Applicant respectfully traverses this rejection since Applicant's admitted prior art is unable to remedy the deficiencies of DeVos pointed out above in conjunction with claims 1-4 and 14-15. That is, Applicant's admitted prior art fails to teach or suggest, *inter alia*, the claimed feature of "inhibiting the signals transmitted from the output line of the second

circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit" (claim 1), or "detecting whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit, and if the receiver-transmitter circuit is transmitting signals to the serial interface circuit, prohibiting the serial interface circuit from transmitting signals to the receiver-transmitter circuit" (claim 15). Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 5-8, 10, 12-13 and 16-18.

Re: Rejection of Claims 8-9 and 19-20

Claims 8-9 and 19-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over DeVos in view of Applicant's admitted prior art, and further in view of U.S. Patent No. 6,639,513 issued to Olsen et al. (hereinafter, "Olsen"). Applicant respectfully traverses this rejection since Olsen is unable to remedy the deficiencies of DeVos and Applicant's admitted prior art pointed out above. That is, Olsen fails to teach or suggest, *inter alia*, the claimed feature of "inhibiting the signals transmitted from the output line of the second circuit to the input line of the first circuit when the first circuit is transmitting signals to the input line of the second circuit" (claim 1), or "detecting whether the receiver-transmitter circuit is transmitting signals to the serial interface circuit, and if the receiver-transmitter circuit is transmitting signals to the serial interface circuit, prohibiting the serial interface circuit from transmitting signals to the receiver-transmitter circuit" (claim 15). Accordingly, Applicant respectfully requests withdrawal of the rejection of claims 8-9 and 19-20.

Conclusion

Having fully addressed the Examiner's rejections it is believed that, in view of the accompanying amendments and remarks/arguments, this application stands in condition for allowance. Accordingly, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at (609) 734-6813, so that a mutually convenient date and time for a telephonic interview may be scheduled. No fee is believed due. However, if a fee is due, please charge the fee to Deposit Account 07-0832.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450 on:

3-9-07 Karen Benbanek

Date